THIN-FILM INTRACORTICAL RECORDING MICROELECTRODES

Quarterly Report #8

(Contract NIH-NINDS-NO1-NS-7-2364)

January – March 1999

Submitted to the

Neural Prosthesis Program
National Institute of Neurological Disorders and Stroke
National Institutes of Health

by the

Center for Integrated MicroSystems
Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, Michigan
48109-2122

April 1999

Thin-Film Intracortical Recording Microelectrodes

Summary

The goal of this contract is to develop a family of active recording probes suitable for fundamental studies in neurophysiology and for use in neural prostheses. The probes will have 64 sites, of which eight can be selected for simultaneous use by the external world. On one of the probe designs (PIA-2B/-3B), the neural signals will be buffered and then passed directly off chip, whereas on the other (PIA-2/-3) the signals will be amplified, multiplexed, and then passed off chip to minimize external leads. Both two-dimensional (2D) and three-dimensional (3D) versions of these probes are being developed.

In this quarter, two active recording probes have been verified electronically and now can be used *in vivo* recording situations. The two probes are the 64-channel front-end-selected probe with 8 channels being delivered off-chip over as many leads and a 64 channel buffered prove with the signals being delivered over parallel leads. A MOSIS chip has been delivered which verifies the design principles of the DC stabilization circuit discussed in the last report. The electrode/tissue-generated offset has been successfully reduced by as much as 60dB by the implementation of a clamping resistance at the input of the buffer stage. This allows large gains in the information containing bands of the neural spike signal while suppressing the DC gain thus allowing the full dynamic range of the communication channel to be utilized. DC suppression will directly effect the SNR of either a time division multiplexer or a quantizer in the last onboard stage of active recording chips. Wireless operation of recording probes continues to be a goal of this program. The various component parts of a wireless system are being designed in detail. This quarter focused on the design of the voltage regulator module of the circuit with simulation of other components underway. We have continued the optimization of the probes for in-vivo use. Recording differences have proven to be minimal among several types of recording sites including gold, Iridium, TiN and conductive polymers. This provides us with an expanded design space to explore the differential ability of different sites to provide long-term recordings. The recording contract in conjunction with one of CNCT's core research project efforts will be working to solve what is now being termed the fouling problem. The current hypothesis is that proteins are being deposited on the recording sites, which result in the reduction of recording amplitude over time.

Thin-Film Intracortical Recording Microelectrodes

1. Introduction

The goal of this program is the realization of batch-fabricated recording electrode arrays capable of accurately sampling single-unit neural activity throughout of volume of cortical tissue on a chronic basis. Such arrays will constitute an important advance in instrumentation for the study of information processing in neural structures and should also be valuable for a number of next-generation closed-loop neural prostheses, where stimuli must be conditioned on the response of the physiological system.

The approach taken in this research involves the use of solid-state process technology to realize probes in which a precisely-etched silicon substrate supports an array of thin-film conductors insulated above and below by deposited dielectrics. Openings in the dielectrics, produced using photolithography, form recording sites which permit recording from single neurons on a highly-selective basis. The fabrication processes for both passive and active (containing signal processing circuitry) probe structures have been reported in the past along with scaling limits and the results of numerous acute experiments using passive probes in animals. In moving to chronic implant applications, the major problems are associated with the probe output leads, both in terms of their number and their encapsulation. The probe must float in the tissue with minimal tethering forces, limiting the number of leads to a few at most. The encapsulation of these leads must offer adequate protection for the megohm impedance levels of the sites while maintaining lead flexibility.

Our solution to this problem has involved two steps. The first has been to embed circuitry in the probe substrate to amplify and buffer the signals and to multiplex them onto a common output line. Using this approach, signal levels are increased by factors of about 300, impedance levels are reduced by four orders of magnitude, and the probe requires only four leads for operation, independent of the number of recording sites. A high-yield merged process permitting the integration of CMOS circuitry on the probe has been developed, and this circuitry has been designed and characterized. The second step has involved the development of silicon-based ribbon cables, realized using the same probe technology, to conduct the neural signals to the outside world. These cables have shown significant advantages over discrete leads, both in terms of the ease with which chronic implants can be assembled and in terms of the ability of the cables to survive long-term biased soaks in saline. The cables can be built directly into the probes so that they come off of the wafer as a single unit, requiring no joining or bonding operations between them. The cables are also significantly more flexible than previously-used discrete wire interconnects.

This contract calls for the development of active probes for neural recording. A 64-site 8-channel probe with site selection and signal buffering but no multiplexing is in development as is a high-end multiplexed version of this device that includes gain. During the past quarter, work concentrated in several areas: 1) the continuation of fabrication of passive probes for internal and external users. We have fabricated a new family of passive probes for general use in addition to a new set custom probes for our closest collaborators.

We continue to evaluate interconnect methods which will lead to easy chronic use of the probes familys; 2) the fabrication of two types of active probes; 3) a fabrication method which can allow an amplifier design which will block DC levels and allow amplification of the neural spike data; and 4) comparative studies of iridium and Ti nitride recording sites. This work is described in the following sections.

2. *Passive System Developments*

2.1 Probe Developments

During the last quarter, 20 wafers of passive probes were processed through the Center for Neural Communication Technology (CNCT). The wafers were from two mask sets: STANDARDS and CNCT4. STANDARDS includes 27 acute and chronic probe designs which are based on design ideas solicited from probe users. These designs comprise the new CNCT catalog that is available for download from the CNCT website (www.engin.umich.edu/facility/cnct). Included are single and multishanked designs suitable for recording and stimulation as well as a few tetrodes. The probes have a standard backend to simplify bonding and pinout maps. A sampling of probes from STANDARDS is shown in Figures 1and 2.

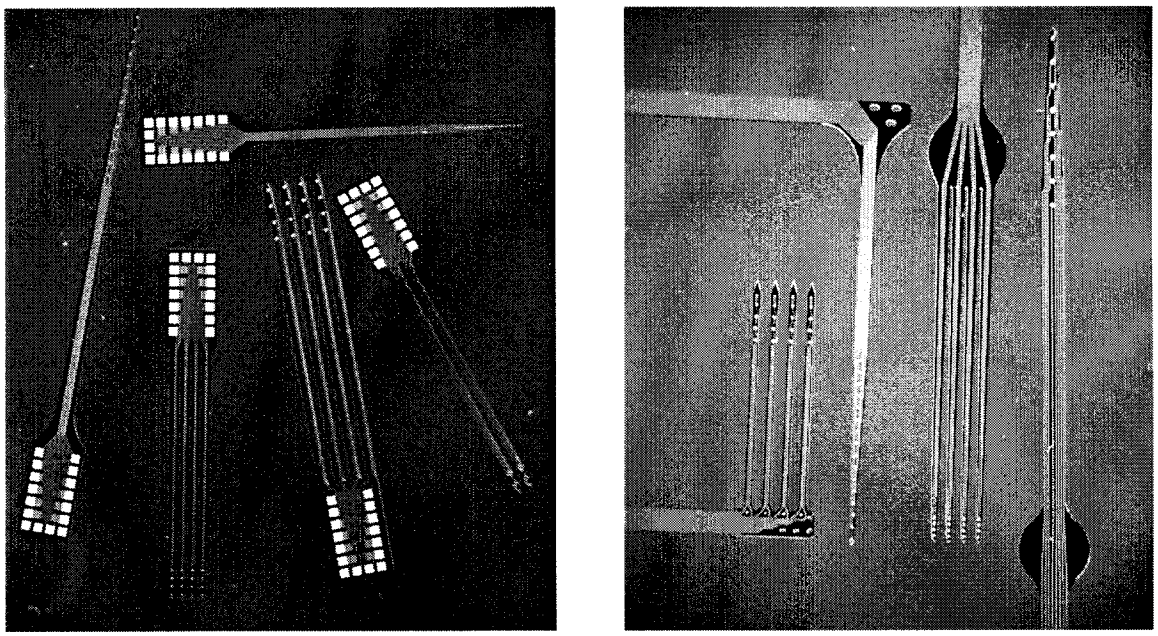


Figure 1: Probes from the new STANDARDS mask set fabricated by the CNCT. These popular designs comprise the new CNCT catalog. In the left photo, acute probes are shown. Sites on the single shank probe on the upper left are spaced on 100µm centers. Chronic probes are shown in the upper right photo, with sites on the probe on the far right spaced on 200µm centers.

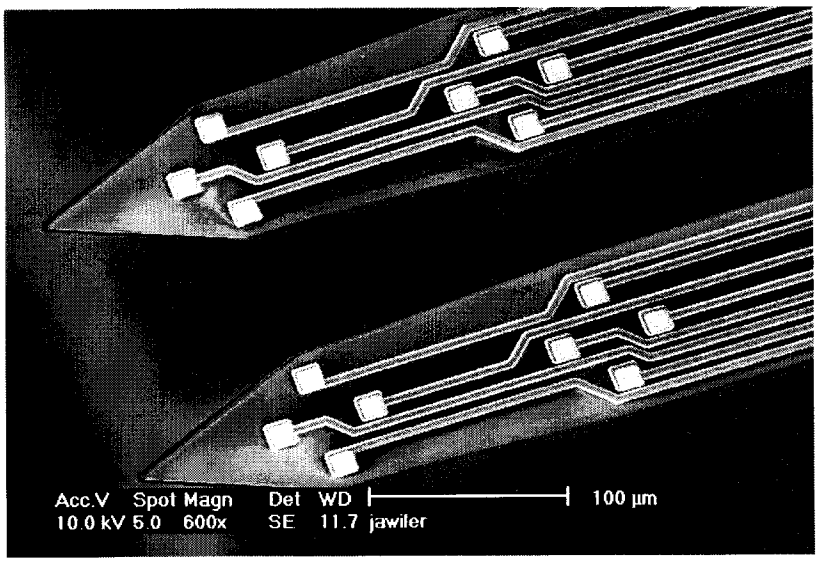


Figure 2: A two shank probe with two tetrodes on each shank.

The CNCT4 mask set is comprised of 22 custom designs submitted by CNCT collaborators and several Neural Prosthesis investigators. Investigators with custom designs on this set include Drs. William Agnew and Douglas McCreery of the Huntington Medical Research Institutes, Dr. David Edell of MIT Lincoln Labs, Dr. Gyorgy Buzsaki of Rutgers University, Dr. James Weiland of Johns Hopkins University, Dr. Wayne Cascio of UNC Chapel Hill, and Dr. John Middlebrooks of the University of Michigan. Figure 3 shows a photograph of some of the designs.

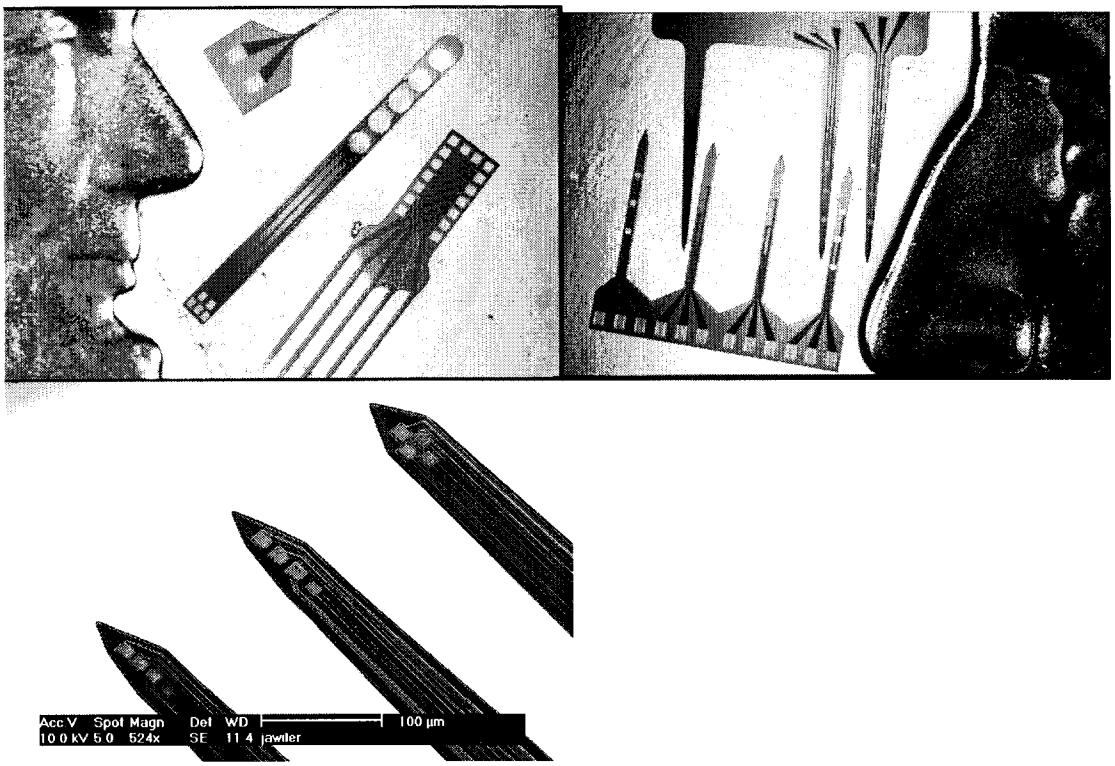


Figure 3: Sampling of probes from the CNCT4 mask set. The middle probe in the upper left photo was fabricated for the Johns Hopkins group for studies of retinal stimulation. The top probe on the upper right was fabricated for Huntington Medical Research Institutes for spinal cord stimulation. The probe in the lower SEM is a three-shank tetrode fabricated for Dr. Buzsaki.

Several new "brain-in-the-box" (BIB) designs with 32 channel capability are also included on CNCT4 and are shown in Figure 4. As described in Quarterly Report #5, the BIB is a 3-D structure constructed from a single cable that forks into two separate probes and are unfolded and inserted into a platform. Different slots in the platform permit a choice of probe spacing. The resulting structure has the site-sides of the probes facing one.

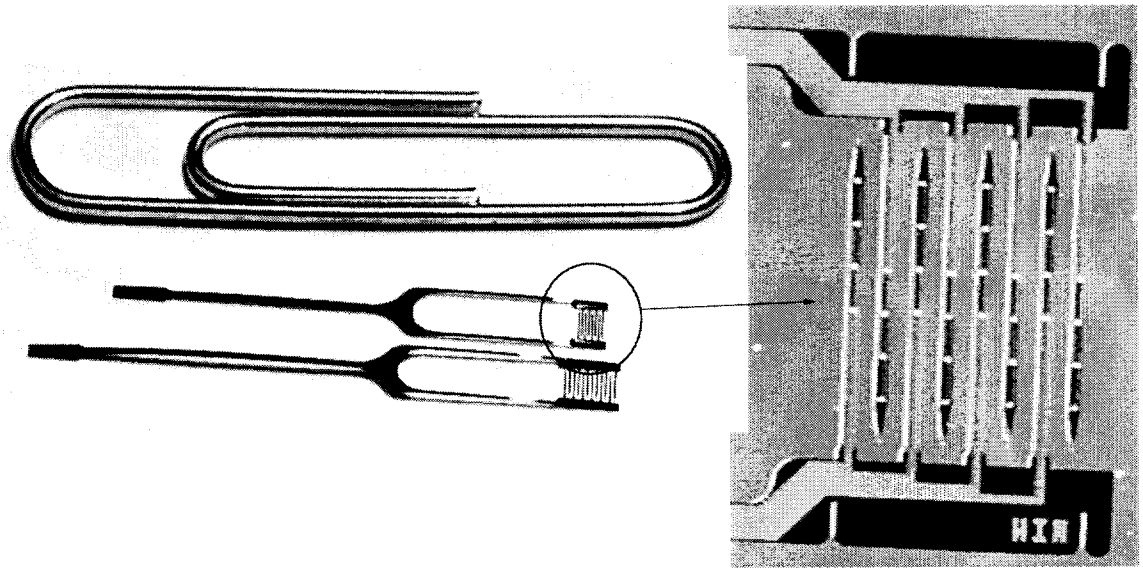


Figure 4: Probes for the new 32-channel brain-in-the-boxes from the CNCT4 mask set.

Versions were fabricated for both guinea pig (shown in blow-up) and cat cortex. Spacers and platforms for each design are also included on the mask set. The shank spacing is 300μm on the guinea pig probe, and 400μm on the cat probe.

2.2 Packaging Developments

In the area of packaging, we have been working to improve our chronic assembly by increasing channel count to at least 16, and improving the mechanical robustness of the interconnect. We have evaluated many commercially available connectors and have found one that appears to be acceptable: the Omnetics NANO connector. The pins are on 0.025" centers which permits a dual-row 18 pin version (16 channels plus grounds) to be realized in a 6.7mm x 1.8mm x 4.4mm package. The connector is quite robust yet has acceptable insertion/withdrawal forces, properties which have been difficult to find in other connectors.

For the interconnect, we have been investigating the use of a hybrid cable. In this scheme, the integrated silicon cable is still used where extreme flexibility is necessary (i.e. from the probe to the supradural space), and an intermediate interconnect is used to take the signals to the percutaneous connector. This scheme permits a reduction in the length of the silicon cable that will in turn increase device yield, and it also allows us to choose a intermediate cable that is mechanically robust.

We have been investigating polyimide cables for the intermediate interconnect. Our first attempt was a commercially manufactured flex circuit from the Dynaflex Corporation, San Jose, CA. This particular cable was found to corrode in soak tests by David Edell of MIT. We have been working with Dr. Edell and Dr. Troy Nagle of the Biomedical Microsensors Laboratory at NCSU on another polyimide cable based on the process presented in a poster at the 1998 Neural Prosthesis Workshop ("Biosensor Flexible Interconnect and Characterization of Flexible Coatings for Long Term Applications," J.

Fiering, S. Ufer, T. Nagle and D. Edell). NCSU has fabricated a cable for us with a 2 mil polyimide substrate, 0.4μm gold leads and a 15μm polyimide top layer. This particular configuration has been shown to perform well under soak, but resulted in a structure that is a bit stiff and warped. We will continue to work with Drs. Edell and Nagle to define a structure that is acceptable in both its mechanical and longterm electrical integrity. Figure 4 shows a mock-up assembly with the Omnetics 18 pin connector and an NCSU polyimide cable.

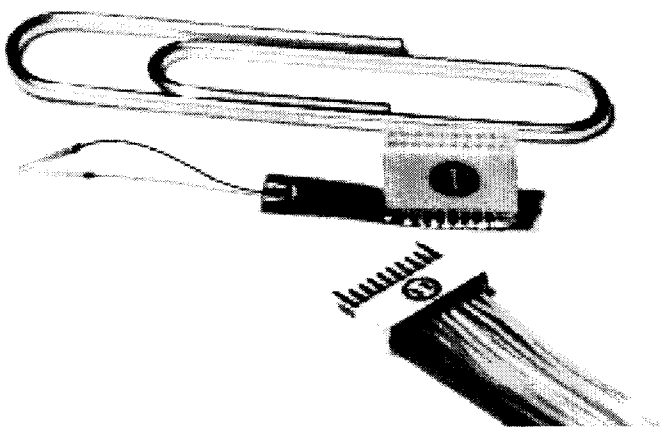


Figure 5: Mock-up of a new chronic assembly being developed. The 18 pin connector is from Omnetics Corp. The interconnect is made up of a silicon cable (in reality, the silicon cable would be shorter) and a polyimide cable fabricated by NCSU. Exposed connections will be insulated with silastic and epoxy. A titanium shell will be added around the connector.

3. Development of Active Recording Probes

3.1 Development of a 64-Site Eight-Channel Non-Multiplexed Recording Proble (PIA-2B)

During the past quarter, fabrication of a 64 site front-end-selected and buffered probe was completed. The architecture and design of this probe have been discussed in previous quarterly reports. Device parameters for the PMOS and NMOS transistors in the CMOS circuitry portion of the probe were given in the last quarterly report. Since this time, the circuits were exhaustively tested and correct functioning was verified. An input clock waveform and the corresponding "I'm OK" signal on the data output pad is given in Figure 6 below. An unbuffered version of the same output pulse is used to latch the serial input into the registers. A serial input data stream and the data register output is also given below.

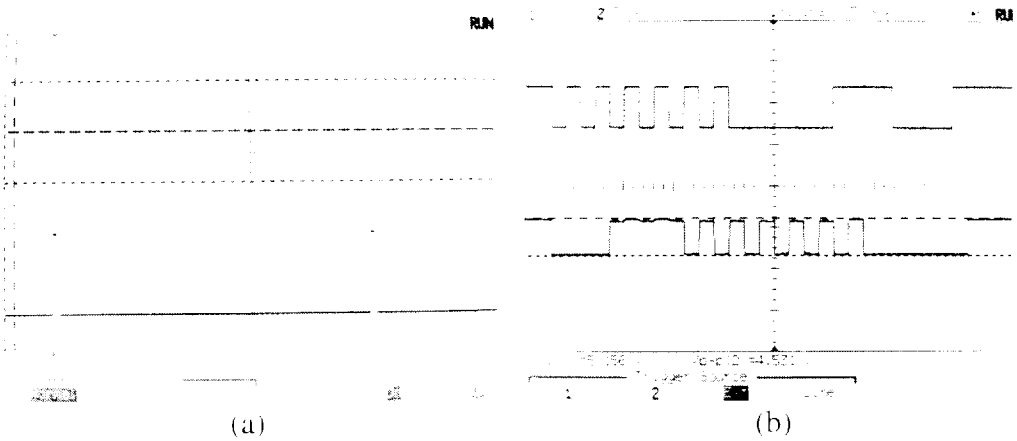


Figure 6: Input and output to selected circuit blocks on PIA-2B. Clock input and resulting output pulse on the data pad is given in (a). Serial data input and register output is given in (b).

After circuit testing, all "post-CMOS" fabrication steps were completed. A frontside dielectric mask to provide protection for the CMOS circuitry during the release of the probes in EDP was designed. This mask uses dielectric bridges and corner compensation to provide etch stops. In addition, masks for second level contacts, sites, pads, and beam-lead electroplating were finalized and fabricated. LTO was deposited on top of the CMOS circuitry to provide a passivation layer, and contacts were cut through the LTO with a dry (RIE) etch. Irridium sites and gold bond pads were deposited, and the field was etched. The wafers are now ready for thinning in HF/Nitric acid and probe release in EDP. A picture of an eight shank chronic probe after all clean room processing (prior to EDP release) is given in Figure 7. The probes will be released from the wafer in the coming days.

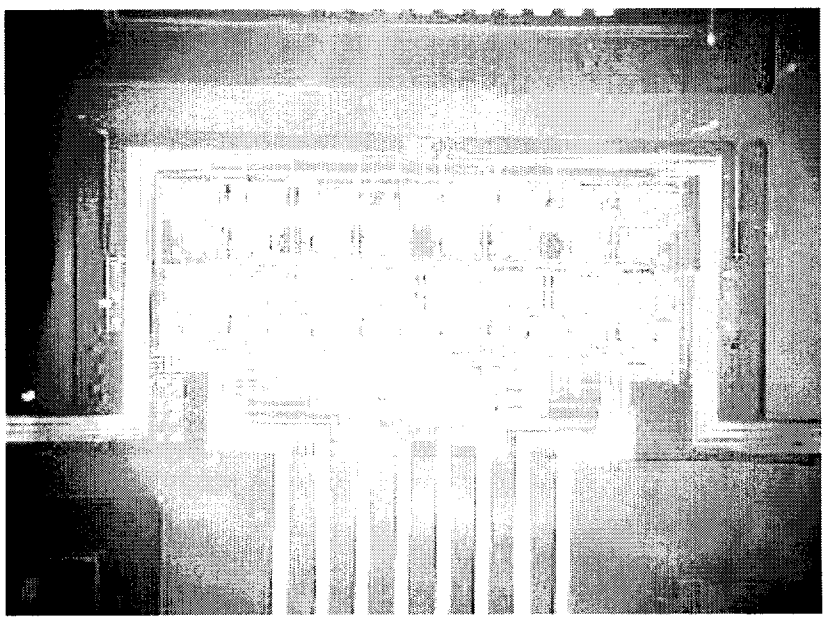


Figure 7: Eight shank chronic probe immediately prior to release from wafer.

After final processing, the CMOS circuits were tested again to verify correct functioning prior to EDP release. All circuit blocks functioned normally, and there was no noticeable difference in yield after these final process steps.

3.2 Development of a 64-Site Amplified and Multiplexed Probe

Work was begun on the design of PIA-2, an amplified and multiplexed 64 site recording probe. To the largest extent possible, PIA-2 (and the 3D version PIA-3) will utilize circuit blocks that have been used successfully on previous probe designs, as shown in Fig. 8 below. These circuit blocks address problems encountered in previous versions of an amplified and multiplexed recording probe, including interchannel crosstalk, drift in the site bias level, and clock feedthrough. The front-end selector circuitry design and layout will be lifted directly from PIA-2b, and the closed-loop amplifier and multiplexer will be that used on the active probes fabricated in 1998 and reported on in previous quarterly reports. The front-end stabilization circuit block used will be the one fabricated at MOSIS and reported on in this quarterly report.

Design work to date has concentrated on verification that the previously measured performance parameters (amplifier current drive, multiplexer sampling rates, etc.) are sufficient for extention to eight input channels. Simulation of the extended circuit blocks has begun. In addition, work has been completed on floor-planning of the layout to minimize layout area. The final design of PIA-2 will be contingent upon any lessons learned in the in-vivo testing of PIA-2b, which will be completed in the coming quarter. In addition, extensive simulation of the circuitry with an emphasis on extraction of parasitic capacitances and resistances from the layout, and the effect of possible process variations on the circuitry will be carried out before fabrication is begun.

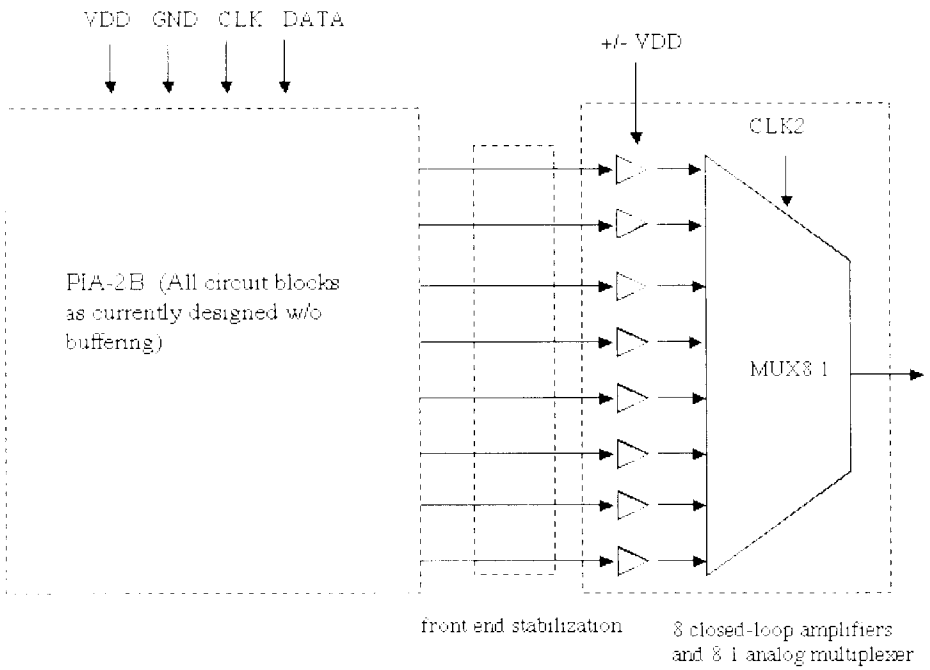


Figure 8: Block diagram of PIA-2 circuitry.

4. DC Stabilization of Electrode Systems

4.1 Design of New DC Stabilization System:

Over the last quarter, a new DC Stabilization system has been successfully fabricated at a VLSI foundry (MOSIS). DC Stabilization involves the rejection of the inherent DC drift associated with the recording of the neural action potential. This DC drift is actually the open-circuit potential of the electrode-electrolyte interface and appears as a "battery" potential at the recording site. Consequently, the action potential can be electrically represented as an AC signal of amplitude ± 150 μV on top of a DC "battery" offset of ± 200 mV. Previous quarterly reports have alluded to the need for developing high-density active probe arrays with on-chip CMOS circuitry for signal processing. However, since the DC potential associated with the recording is about 1000 times larger than the AC signal to be recorded, it is necessary to lower the gain of on-chip circuitry to prevent saturation of the system. Thus, the gain of all circuit blocks in the system becomes limited by the DC offset which is highly undesirable. Furthermore, any signal processing scheme (such as analog to digital conversion) requires a stable DC baseline in order to ensure efficient operation. Thus there is a need to clamp this battery potential to ground at the front-end of the probe without sacrificing the AC performance (i.e. the actual recorded action potential).

In earlier designs, DC stabilization was achieved by a variety of methods including diode clamps, reset gates etc. However, none of them proved to be completely satisfactory. The reset gate circuit (where an input transistor was periodically turned on in a frame interval to clamp the input node) suffered from the problem of clock feedthrough noise coupling into the amplifier system which had a detrimental effect on the rest of the system. Diodes on the other hand suffered from the serious problems of optical drift. Illumination of the silicon wafer results in optically based charge carrier generation. These charge carriers result in optical polarization currents (which are typically tens of picoamps) that result in an offset of the I-V curve of the diodes. Also, the resistance of reverse biased diodes is much higher than that needed, especially for optical currents. The maximum polarization currents needed to clamp the battery is about a picoamp while the optical currents are typically tens of picoamps. Thus input diode clamps proved to be unsatisfactory and a new method was required.

It is well known that the ideal method to DC stabilize a recording site is to use a resistive clamp at the input of the amplifier. The main constraints that the determine the choice of the resistor value are: 1) clamping the DC potential reliably, and 2) ensuring that the AC cut off frequency does not rise above 100 Hz.

Typically, for conventional values of electrode resistance, and capacitance, the optimum value of the resistance is about 80 MΩ to 300 MΩ. Such a high value of resistance cannot be easily realized with thin film resistors due to the area that the resistor would occupy.

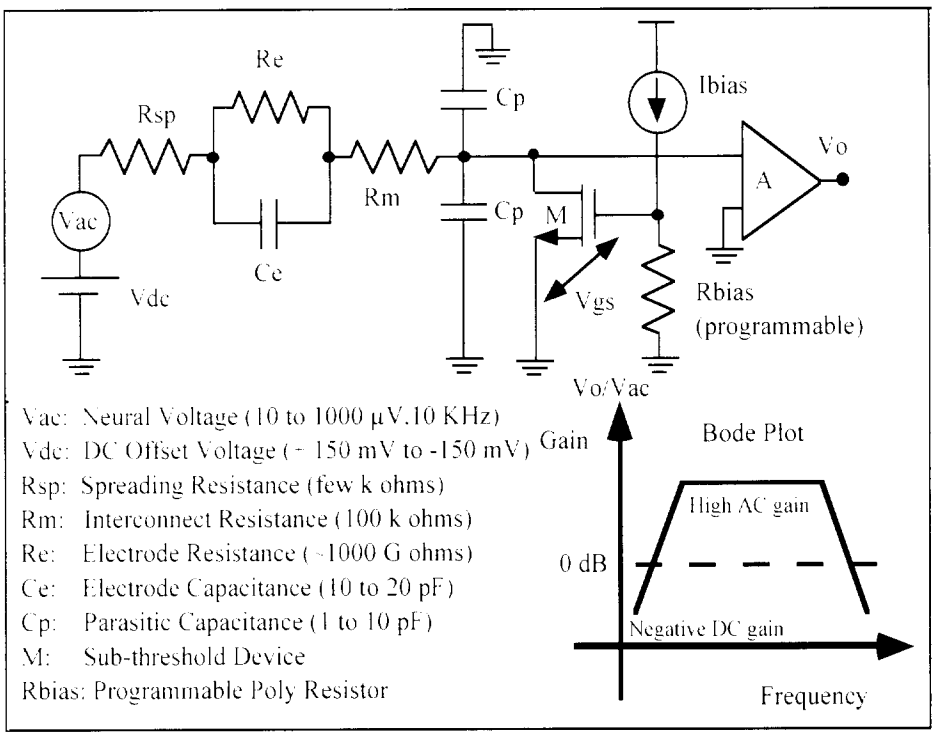


Figure 9: Representation of the electrode-electrolyte interface and the DC stabilization system.

Figure 9 above, shows the electrical model of the recording interface along with the newly developed DC stabilization system. The DC suppression in this system is brought about by the front–end NMOS transistor M. This transistor is biased by the current I_{bias} that is passed through the resistance R_{bias}. R_{bias} can be trimmed with a laser to modify the bias on the transistor M. M is designed to be biased in the subthreshold regime ($V_{gs}<V_t$). In the subthreshold regime, the NMOS transistor essentially behaves as a bipolar junction transistor (BJT) with an exponential I-V law. The main feature of interest is that in the sub-threshold region, large resistances can be obtained with a very small area (essentially the area of the device itself). Since the I-V relationship is exponential, the resistance offered by M can be adjusted by an order of magnitude by modifying the gate bias (V_{gs}). Thus, M now behaves as if it were a large resistive clamp at the input node of the amplifier. However, the attractive feature in this new system is that the new resistance is:

1. Voltage controlled
2. Low area
3. Relatively insensitive to optical currents.

The DC performance of this system is set by the resistive divider formed between the electrode resistance R_e, and the drain-source resistance of M (R_{ds}). The AC performance of the system is set by the high-pass filter formed between the electrode capacitance C_e and R_{ds}. By biasing transistor M, in the subthreshold region, it is possible to obtain large resistances to the order of 100 MΩ to 1 GΩ which are optimal to clamp DC drift by resistive divider action. Also, since the resistance of the transisitor M (R_{ds}) is large, the cut off frequency of the C_e-R_{ds} high pass filter, does not compromise AC performance. The DC Stabilized signal is amplified by an amplifier (A). This amplifier is implemented as a 4-stage circuit employing DC feedback to attenuate any residual DC drift seen at the input node and is quite similar to earlier designs fabricated at the University of Michigan.

4.2 Fabrication of DC Stabilization System

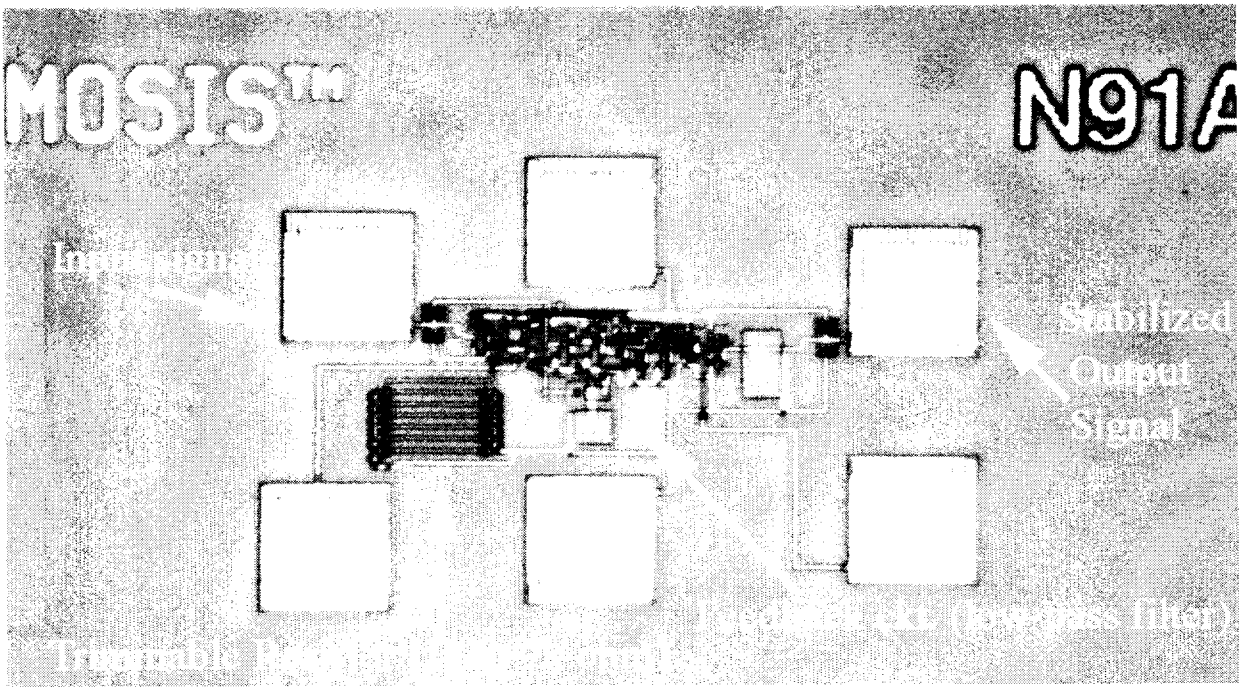


Figure 10: DC Stabilization-Amplifier System fabricated at MOSIS in 1.2 μm CMOS.

Figure 10, above shows a die photograph of the above mentioned DC stabilization –amplifier system, fabricated at MOSIS in a 1.2 μm, n well CMOS process.

4.3 Test Results From the DC Stabilization System:

The fabricated circuit was extensively tested, on the bench as well as with iridium recording electrodes in saline. The table below shows some of the measured results.

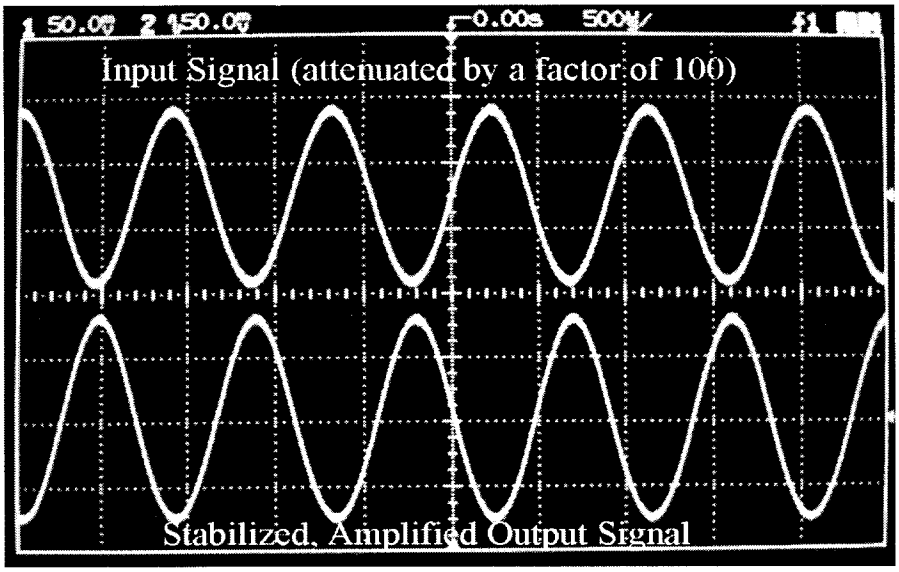
SPECIFICATION	**MEASURED VALUE**
Maximum Mid-band Gain	42 dB
Lower Cut-off Frequency	20 Hz
Power Dissipation	~150 μW
Tolerable DC (Input) Offset Range	400 mV

Table 1: Measured Results of the DC Stabilization System

It must be noted that the measured values were slightly different from those obtained through HSPICE simulations due to a threshold shift of 21 % on the NMOS transistors. This

problem was somewhat overcome, by changing the power supplies and trimming the biasing resistance R_{bias} which altered the bias on the front-end transistor M.

DC and AC tests: The most important tests that can be performed on a system of this type are DC and AC tests with iridium based passive recording probes in saline. The results of these are shown below.



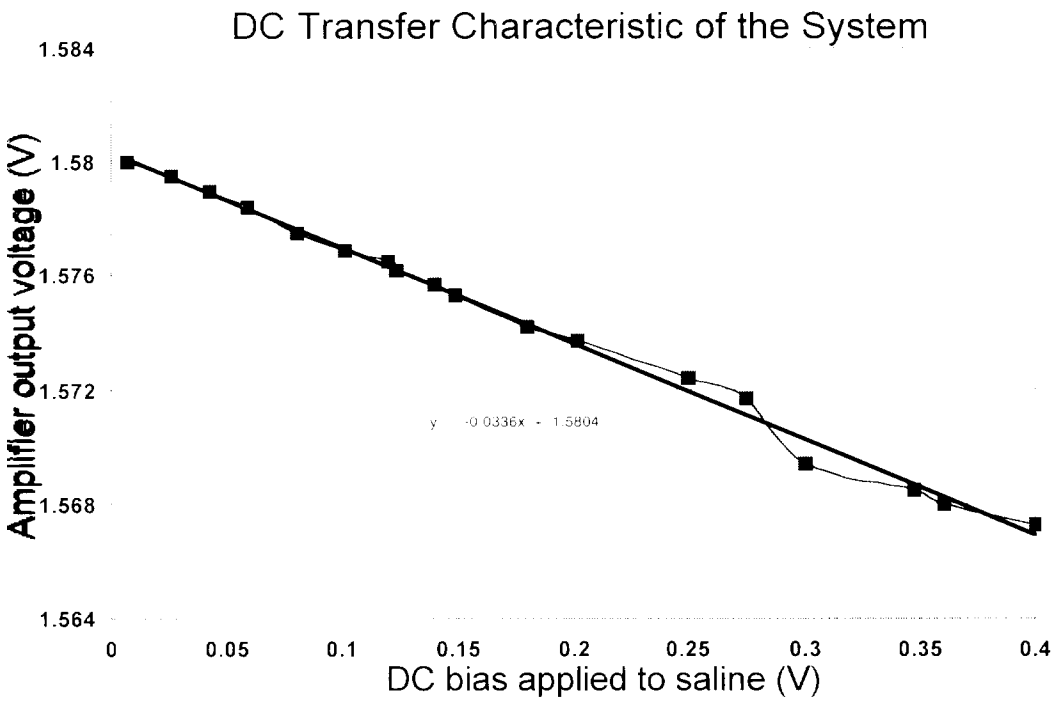


Figure 11: DC and AC performance of the system with a 16 site recording system in saline.

Figure 11 shows the performance of the DC stabilization-amplifier system with iridium recording sites in saline. The saline solution is driven with a sinusoidal signal which is attenuated by a factor of 100 in order to obtain signals of amplitude in the microvolt range. The AC performance is seen in the top plot which shows the photograph of the oscilloscope with the input and output channels at a frequency of about 1 kHz. The top channel shows the input signal (that is attenuated by a factor of 100) and the bottom channel shows the amplified output of the amplifier.

The lower curve conveys information about the DC behavior of the system which is a more important test. The vertical axis represents the DC output level of the amplifier, while the horizontal axis shows the DC bias on the saline. It can be seen that the DC level of the output signal is almost constant even with a 400 mV bias applied to the saline solution. The plot shows a linear fit to the obtained data points indicating that the amplifier is in the linear region of its characteristic and has not saturated even at a high input DC bias. The slope of the linear fit to the curve indicates the DC gain of the system and it can be seen that the DC attenuation is about –30 dB. Moreover the DC attenuation is the same in lighted and dark conditions indicating optical effect insensitivity. Although the value of DC attenuation is less than that obtained through simulations, it is believed that the variation is due to process drifts mentioned earlier.

In such tests, it is necessary to ensure that the DC bias that is being applied to the saline is indeed the DC bias that is reaching the stabilization circuit. In order to test this, the stabilization-amplifier system was removed, and the saline was biased to different DC potentials. The saline potential was recorded by studying the DC output of a CMOS buffer whose input was connected to the iridium electrode. Since the buffer has a gain of 1, the change in the output DC level is equivalent to the potential reaching the DC stabilization stage at a particular saline bias voltage.

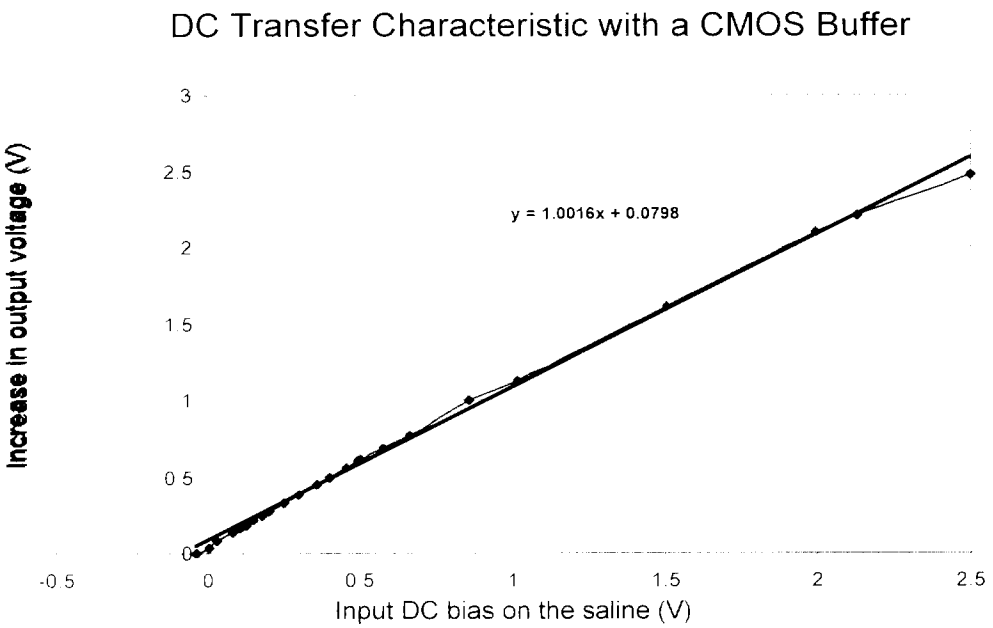


Figure 12: DC Transfer curve (with a linear fit) for a CMOS buffer output.

Figure 12 shows a plot of the output of the buffered system with a linear fit to the curve. The slope of the line is 1.0016 indicating that the relationship between the applied saline bias and the DC level of the output (i.e. the DC bias reaching the stabilization-amplifier system) is linear. This plot indicates that the applied DC bias on the saline is reaching the DC stabilization circuitry and is indeed being significantly attenuated. It thus reinforces the reliability of the results depicted in Fig. 3 earlier.

5. *Telemetry System Design:*

Over the last quarter, work has begun on the design and simulation of the telemetry platform for the wireless operation of neural recording probes. The aim of such a system is to develop a "Subdural Telemetry Platform" that contains the necessary circuits and electronics for on-chip signal processing and control. While the final goal of such a system is to control an array of active probes, for the present it is felt that the telemetry design should be for a passive probe. This step will enable a better understanding of some of the critical issues involved such as the trade off between power and bandwidth and the issue of increased resolution impacting the data transmission rates. The representation of the proposed telemetry platform is shown below.

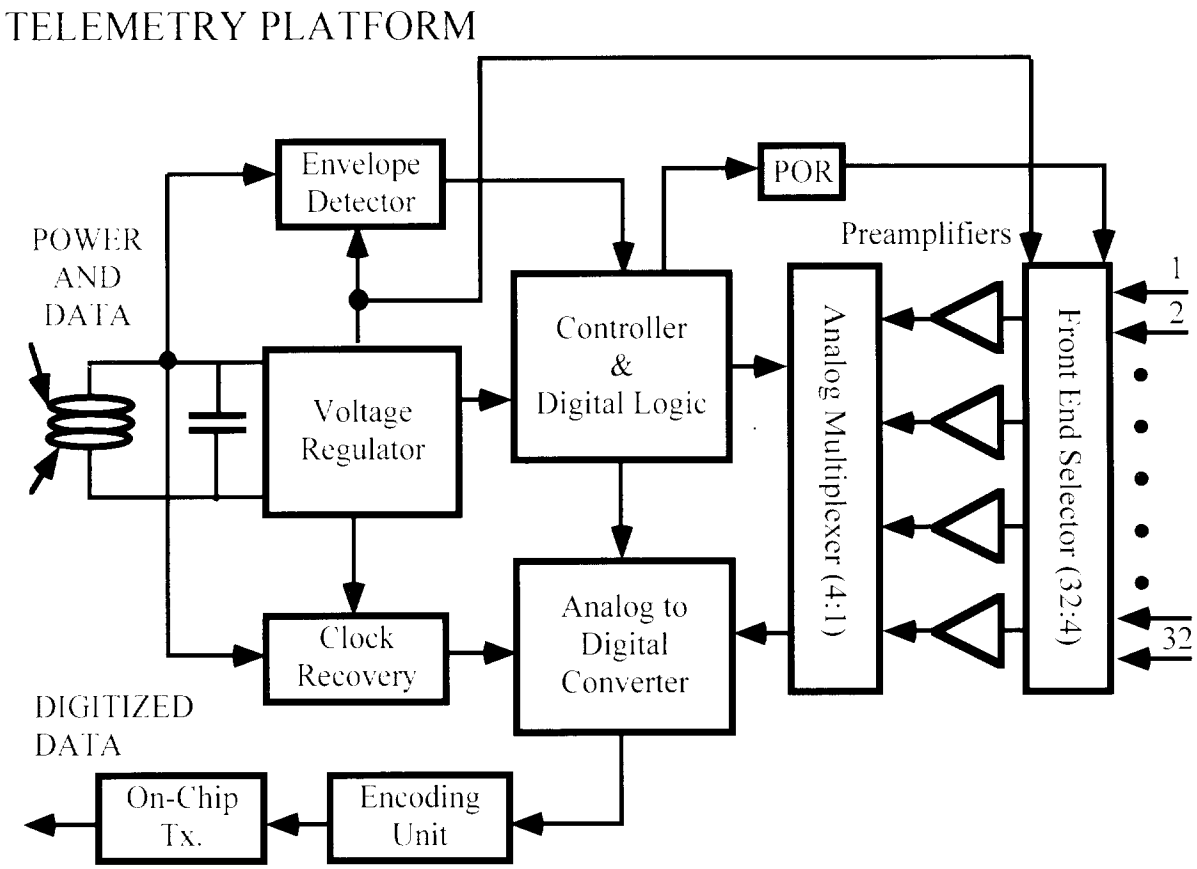


Figure 13: Proposed implementation of the telemetry platform.

Figure 13 indicates the main circuit blocks of the system. It is desired to operate the circuit from an external interface that consists of a Class E amplifier which supplies RF power and data to the system. The RF signal is captured, rectified and demodulated to obtain the necessary power and control for the system. The recorded, stabilized and amplified signal is multiplexed and digitized before being transmitted out to the external interface.

Table 2 below shows some of the important circuit specifications.

SPECIFICATION	VALUE
FREQUENCY (FORWARD)	4 MHZ
FREQUENCY (REVERSE)	> 25 M HZ
TYPE OF PROBE	32 SITE (PASSIVE), 4 CHANNELS SELECTED
RANGE OF OPERATION	~1 cm
TECHNOLOGY TO BE USED	1.2 µM CMOS

Table 2: Specifications of the proposed telemetry system.

Design of Voltage Regulator:

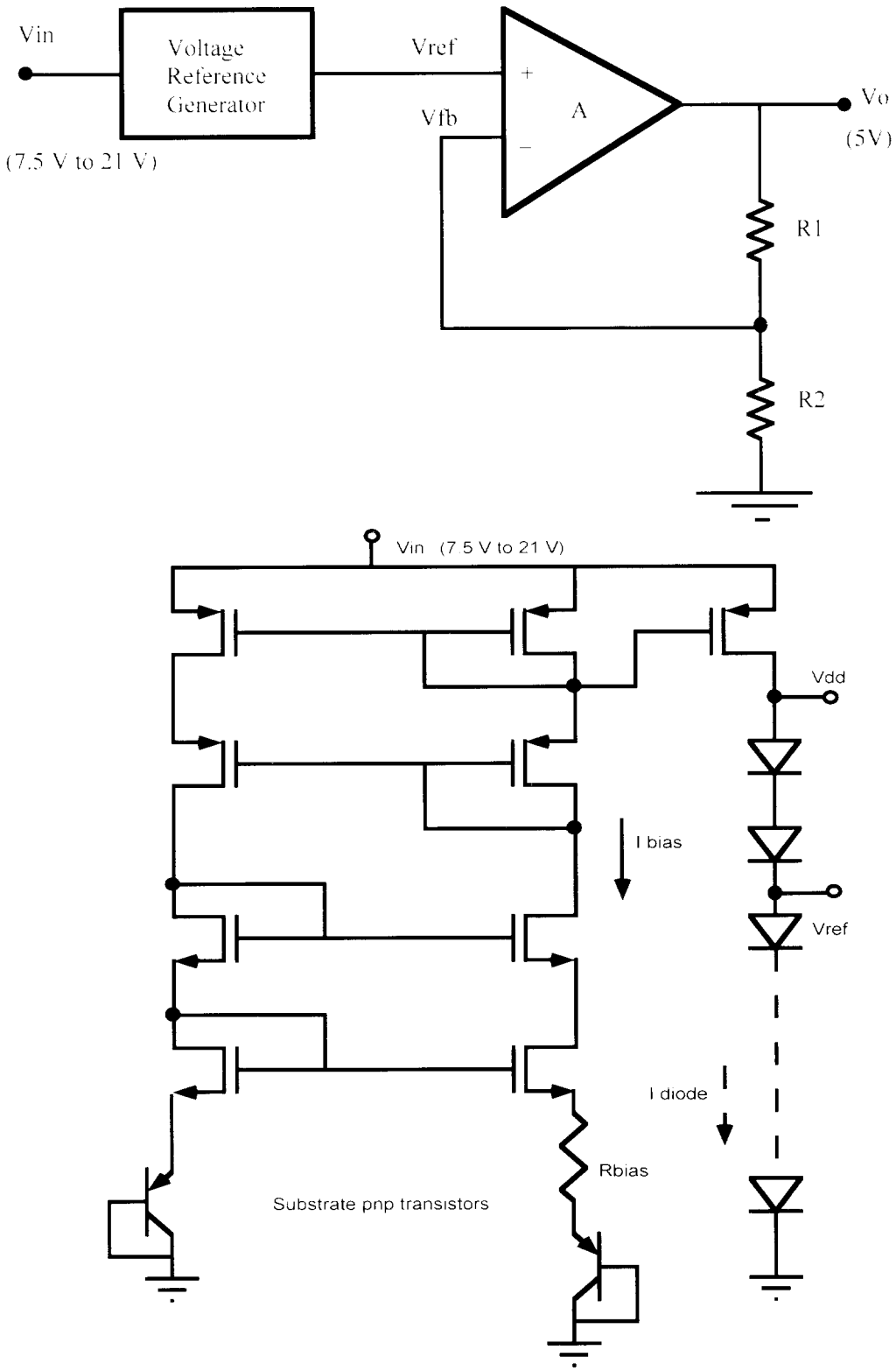
As mentioned earlier, the design and simulation of the above telemetry platform circuit blocks has begun. The Voltage regulator has been designed and simulated in HSPICE. The circuit works well, producing a 5 V output signal for an input rectified signal varying between 7.5 V and 21 V. The system dissipates 5 mW of power at 7.5 V. The circuit implementation is shown in Figs. 6 and 7 below. The regulator is realized as a 2-stage circuit. The input signal drives a supply independent current source (shown in Fig. 7). The current flowing in the current source is given by the ratio of the differences in the base emitter voltages of the substrate pnp transistors and the resistance R_{bias}. Thus,

$$I_{bias}=I_{diode}=\Delta V_{be}/R_{bias}$$

To first order, the current in the diode string, I_{diode} is independent of supply variations and is used to generate a voltage reference Vref. Vref is then supplied to the non-inverting circuit consisting of the opamp and the resistors R1 and R2. Thus the output voltage now only depends on V_{ref}, R1 and R2 all of which are constant. Thus V_0 is given by,

$$V_0=V_{ref}(1+R1/R2)$$

The voltage regulator is especially important in the telemetry circuit because its stability will directly impact the resolution of the ADC.



Figures 14 and 15: Diagram of a 2-stage voltage regulator and reference voltage generator.

Conclusions and Goals for the Forthcoming Period:

Over the last quarter, the following tasks have been performed:

1. Fabrication, testing and calibration of DC stabilization system.
1. Design work on the telemetry platform for wireless operation of neural recording probes.

Over the next quarter, the following tasks have been proposed:

1. Completion of design of telemetry system
1. Fabrication and testing of the telemetry system

Initiating another fabrication run of the new DC stabilization technique with some modifications such as using a closed loop preamplifier etc.

6. Comparison of Recording Site Materials

During this past quarter, we have started to compare various recording site materials for use in chronic preparations, in an attempt to extend the length of time that we can record from a given animal.

The use of an electrode site material containing a high-density of micropores can greatly increase the effective surface area of the site and its associated capacitance, resulting in low impedance and high charge-transfer capabilities. Titanium nitride (TiN) thin film sites sputtered at 70° [1] in a nitrogen/argon atmosphere have been reported [2]. In this work, we have incorporated TiN sites into a full probe fabrication sequence and are now performing detailed comparisons with sputtered activated iridium electrodes.
Silicon microprobes were fabricated using a boron etch stop process up to the point of site deposition. Then, sputtering in a 50% nitrogen/50% argon atmosphere at 7mTorr was used to deposit the TiN sites.

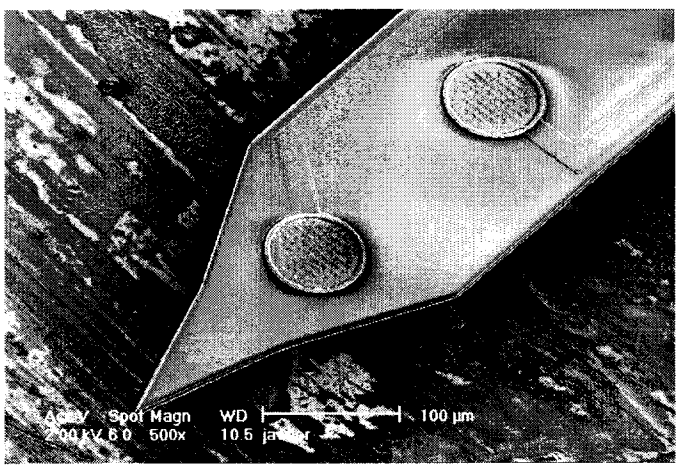


Figure 16: SEM of a TiN site, SX04 electrode.

Figure 16 shows that the sites have been found to be fully compatible with the probe process, with clean lift-off even when deposited using low grazing-angle sputtering. The wafers were oriented normal (perpendicular) and at 70° incidence angle (tilted) to the wafer during

sputtering. Lift-off was then used to define the sites, and wafer processing was completed with a release etch in ethylenediamene pyrocatechol (EDP).

Figure 17 shows the sectioned sites, revealing a porous and highly columnar film structure, which can increase the effective surface area of the site. The figure on the left is that of TiN sputtered at 70° angle of incidence (tilted) and the figure on the right was sputtered perpendicular to the wafer surface (normal). Titanium nitride has the characteristic of being highly columnated, which may result in a better neural tissue interface than iridium.

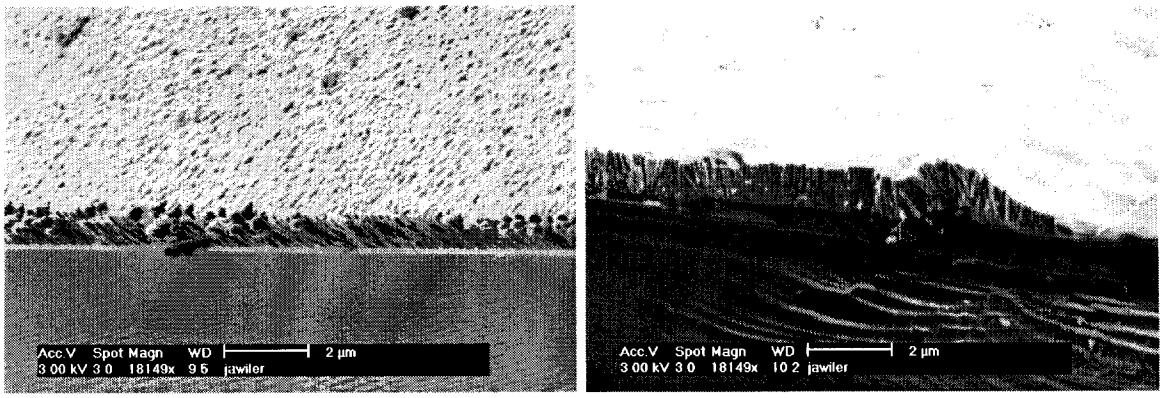


Figure 17: SEM of cross-sectioned TiN sites, the figure on the left was sputtered at 70° and the figure on the right was sputtered at 90°.

Cyclic voltametry (CV) and impedance spectroscopy were conducted on the finished devices. We may expect that TiN is different from Ir in that it does not have any chemical changes during the CV cycles. Impedance spectroscopy (Figure 18) indicates tilt-sputtered TiN has the lowest impedance at 1kHz and at low frequency TiN mainly has a capacitive effect since the phase almost goes to -90°. This also verifies the expectation from the CV cycle: i.e. chemical changes may happen at the site surface during the electric charge exchanges.

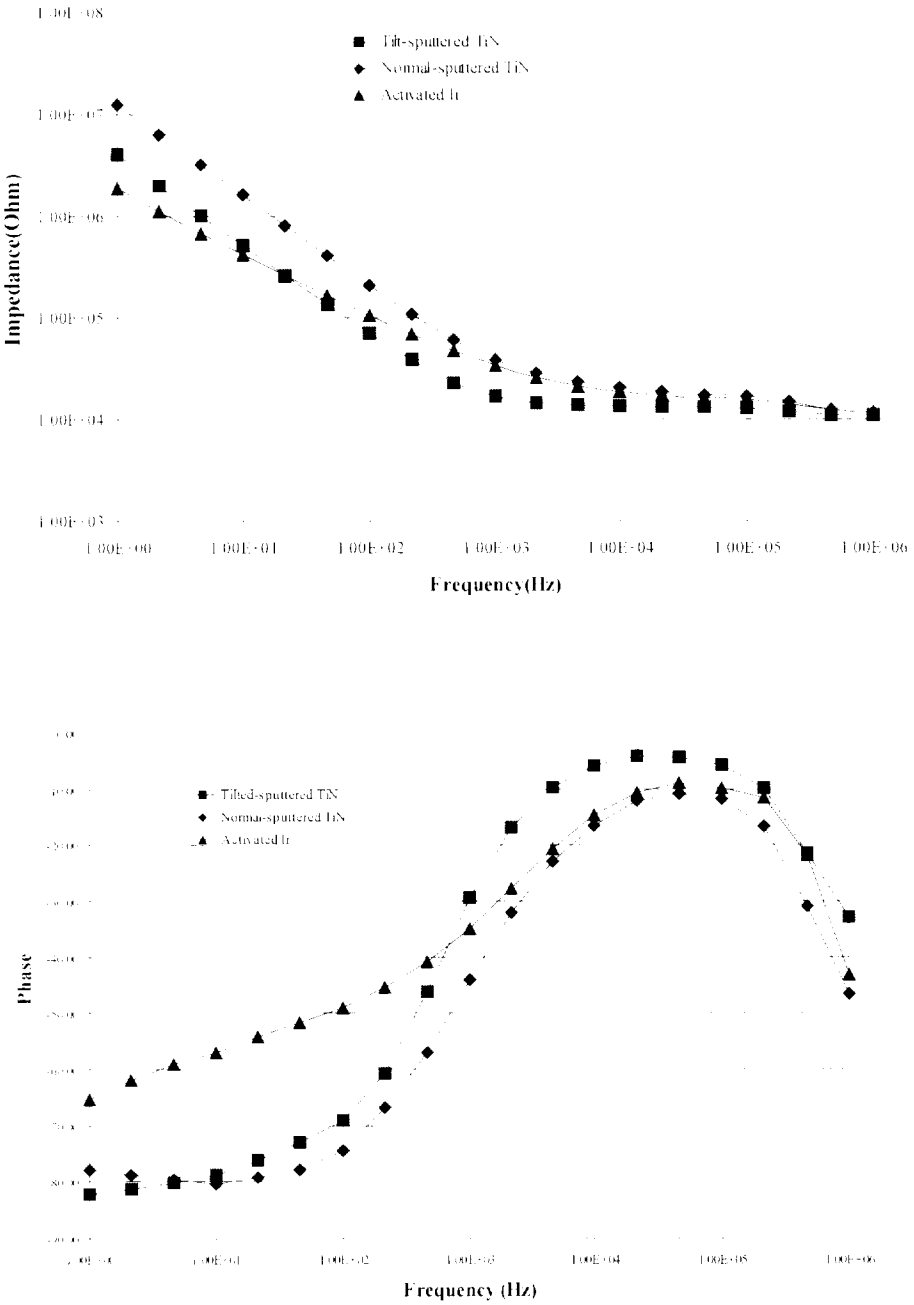


Figure 18: Impedance (top) and Phase (bottom) plots of TiN and Ir.

Another site material we are looking at is polypyrrole deposited over iridium sites. Polypyrrole is a conductive polymer which starts out flat, but as it is deposited, small fingers grow off of the surface which will collapse if too much is deposited (Figure 19). It is these fingers which may help it integrate better into the neural tissue.

Figure 19 is an example of acute recordings obtained from guinea pig cerebellum with iridium: polypyrrole coated iridium and a titanium nitride sites. There is virtually no difference in the signal-to-noise ratios among the different site materials.

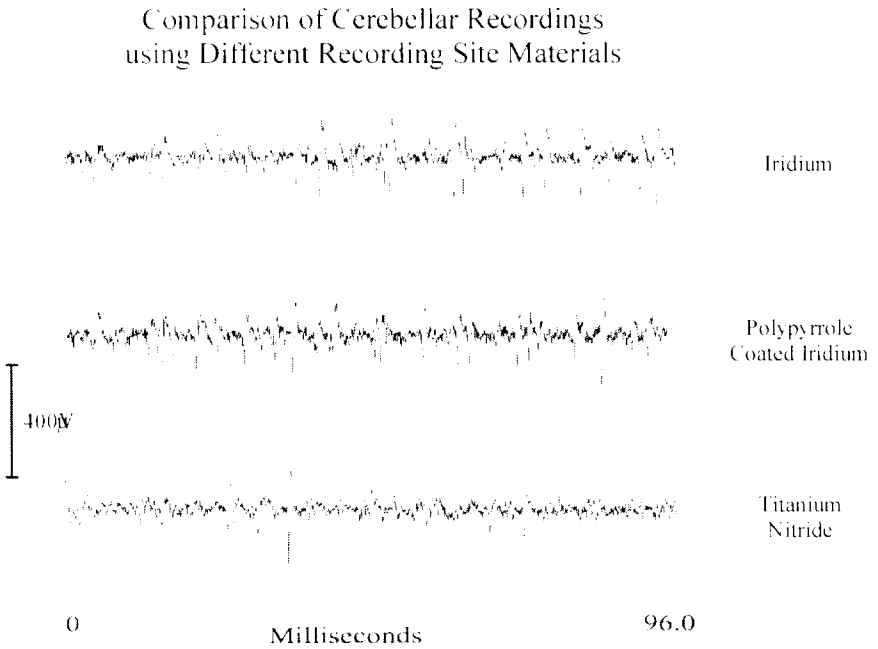


Figure 19: Comparison of Guinea Pig Cerebellar Recordings using Iridium, Polypyrrole Coated Iridium and Titainium Nitride Recording Site Materials.

The next step that we are going to take is to use these site materials in chronic preparations. We hypothesize that by modifying the surface structure of the site in contact with the neural tissue to a more neuron friendly morphology we may reduce the depositoin of get less tissue reaction to the electrode and thus record for longer time frames.

We are also looking into the use of TiN as a stimulating electrode material and are doing tests to determine its charge delivery capabilities.

REFERENCES

[1] J. Thornton, "The Microstructure of Sputter-deposited Coatings,"*J. Vac. Sci. Technol.* A4(6), p. 3059-3065, Nov/Dec 1986.

[2] M. Janders, U. Egert, M. Stelzle, "Novel Thin Film Titanium Nitride Micro-electrodes with Excellent Charge Transfer Capability for Cell Stimulation and Sensing Applications," *Proc. 18th Annual Int. Conf. IEEE EMBS*, Amsterdam, The Netherlands, 1996, ISBN 90-901005-9 (CD-ROM) #364.